CALL FOR PAPERS

The Leading International Components, Packaging, and Manufacturing Technology Symposium

IEEE CPMT Symposium Japan 2018

November 19 – 21, 2018,
Kyoto Univ. Clock Tower Centennial Hall, Kyoto, JAPAN
http://www.ieee-csj.org/

"Electronics Packaging toward Singularity"

"IEEE CPMT Symposium Japan (ICSJ)" is a widely-recognized international conference of the **IEEE EPS Society**, held annually in Kyoto in November. The conference originally started in 1992 as "The VLSI Packaging Workshop in Japan", and was re-named to "ICSJ" in 2010. ICSJ will provide a platform for you to communicate and interact with global leaders in packaging technology.

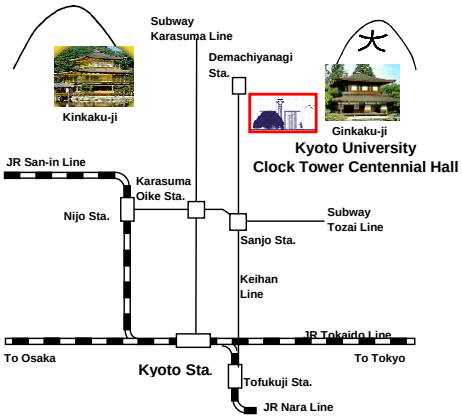
Electronics Packaging toward Singularity: For many decades the number of transistors in a semiconductor chip have increased double every 18 months as Moore's low predicts. In generic perspective the exponential growth of the world's information and the Internet of Things (IoT) will lead to the "Technological Singularity" point at which Artificial Intelligence (AI) has more power than human beings in every aspect. This conference will picture the future state of the electronics packaging which impacts the infrastructures of IoT, AI, deep learning and robotics, and try to predict where the packaging technology is heading. This poses a major challenge for us to determine what our role in the society would be before the Singularity. In 2018, the conference will emphasize the following main topics: **Optoelectronics, Advanced Packaging, Power Electronics & Automotive, Bioelectronics,** and **Thermal Management**. Additional topics of primary interest to the participants are listed below.

Other topics include (but not limited to):

+ 3D Packaging & Chip on Chip
+ Advanced Fine Pitch Packaging, Micro Bumping, Wafer Level CSP
+ Board-Level Integration & Integrated Substrate
+ Laminated Materials & Processing, Materials for Packaging
+ Reliability & Failure Mechanisms
+ Packaging for High-Speed Electrical Interconnect
+ Signal Integrity / Power Integrity
+ RF Components & Modules (w/o mainly Circuit nor Chip)
+ Additive Manufacturing, 3D Printed Electronics
+ Brain-like Neuromorphic Chip Assembly
+ Resilient Packaging for Autonomous System
+ Low Power / Low Temperature / Ultra Low Noise System Packaging

Bring your latest research results, share them with experts from industry and academia, and discuss your work with them. Anybody in the field of the packaging technologies is very welcome to present their latest accomplishments and participate in the discussion. The conference will provide a perfect opportunity to communicate, interact, and exchange technical idea. Young researchers within 2 years' experience in their professions and all students including Ph.D. are also welcome to the newly planned poster session

called “Early Career Researcher’s (ECR) session” for their start-up to the technical presentation and fruitful communication with experts. Authors are invited to submit an abstract through our web site, http://www.ieee-csj.org. **The abstract deadline is ~~May 25~~ (Extended) June 15, 2018**. Acceptance notifications will be sent by July 6, 2018. Accepted authors are requested to submit the manuscript by September 7, 2018 for the Technical Digest, which will be available via **IEEE Xplore**. 4-page manuscript is required for the regular session, while 2-page manuscript is enough for ECR session.



Plenary & Special Speakers

Plenary Speakers

Toru Baji (NVIDIA)

Clint Schow (University of California, Santa Barbara)

Daniel Kuchta (IBM T. J. Watson Research Center)

Amin Shokrollahi (Kandou BUS)

Singularity Special Speaker

Shintaro Yamamichi (IBM Research, Tokyo)

EPS Special Speaker

Chris Bailey (University of Greenwich)

EPS Lecture Event Speaker

Mudasir Ahmad (Cisco Systems, Inc. San Jose)

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